# INTEGRATED LOGIC AND LATCH DESIGN WITH CLOCK GATING AT STATIC INPUT SIGNALS

ABSTRACT

A method and an apparatus are provided for implementing a logic circuit with integrated logic and latch design. A clock input is provided to the logic circuit. One or more static signal inputs are further provided to the logic circuit. One or more dynamic signal inputs are generated by dynamically gating the one or more static signal inputs with the clock signal. The one or more dynamic signal inputs are applied to the logic circuit, and one or more dynamic signal outputs of the logic circuit are generated. The one or more dynamic signal outputs are precharged, and the one or more dynamic signal outputs are evaluated. The one or more dynamic signal outputs are held when the one or more dynamic signal outputs are neither being precharged nor being evaluated. The one or more dynamic signal outputs are converted into one or more static signal outputs.